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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,225	04/13/2004	Brian T. Edgar	STL11600	4622

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EXAMINER	
TRUONG, LOAN	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 10/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/823,225	EDGAR ET AL.	
	Examiner	Art Unit	
	LOAN TRUONG	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/13/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6, 9-13, 15-16 and 19-22* is/are rejected.

7)☒ Claim(s) *5,7,8,14 and 17-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 5, 7-8, 14 and 17-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-4, 6, 10-13 and 15-16 are rejected under 35 U.S.C. 102(a) as being anticipated by Singh et al. (US 6,484,276).

In regard to claim 1, Singh et al. disclosed a method comprising the steps of:

receiving a command at a device through a sequencer that controls interactions on a small computer system interface bus (*fault injection run, fig. 6a, 607)*;

programming the sequencer to interrupt a co-processor before executing the command (*plugin can be integrated into another program an executed from that program, col. 3 lines 30-34);* and

executing a set of instructions on the co-processor based on a stored error mode page so that a false error condition is generated (*fault injection run on target machine, fig. 5 and fig. 6A).*

In regard to claim 2, Wolin et al. disclosed the method of claim 1 wherein executing a set of instruction comprises reprogramming the sequencer so that it is prevented from entering a reselection phase to re-establish a connection across the small computer system interface bus (*GW determines what programs needed to be started on the target machine to create the desired workload, col. 8 lines 45-50, fig. 6a).*

In regard to claim 3, Singh et al. disclosed the method of claim 2 wherein preventing the sequencer from entering a reselection phase comprises preventing the sequencer from entering a reselection phase to re-establish a connection to transfer data (*GW determines what programs needed to be started on the target machine to create the desired workload, col. 8 lines 45-50, fig. 6a).*

In regard to claim 4, Singh et al. disclosed the method of claim 2 wherein preventing the sequencer from entering a reselection phase comprises preventing the sequencer from entering a reselection phase to re-establish a connection to transfer a status after allowing the sequencer to transfer data (*GW determines what programs needed to be started on the target machine to create the desired workload, col. 8 lines 45-50, fig. 6a).*

In regard to claim 6, Singh et al. disclosed the method of claim 1 wherein executing a set of instructions comprises replacing the command with an illegal command (*FIIntercept:inject(), fig. 2b).*

In regard to claim 10, Singh et al disclosed a device comprising:

a sequencer adapted to be connected to a small computer system parallel interface bus (*WGRemote, fig. 5, 50)*;

a co-processor (*target machine, fig. 5, 501)*, coupled to the sequencer and capable of being interrupted (*stopping the workload process, fig. 3c)* by the sequencer and of providing instructions to the sequencer (*WGRemote, fig. 5, 50)*; and

an instruction storage component (*data collection class control flow, fig.* communicatively connected to the co-processor (*target machine, fig. 5, 501)*and containing processor-executable instructions that are designed to initiate an error condition (*fault injection run, fig. 6a)* after the sequencer sends an interrupt (*plugin can be integrated into another program an executed from that program, col. 3 lines 30-34)* to the co-processor (*target machine, fig. 5, 501).*

In regard to claim 11, Singh et al. disclosed the device of claim 10 wherein the processor-executable instructions comprise instructions for preventing the sequencer from entering a reselection phase for a period of time so that the sequencer does not establish a connection across the small computer system parallel interface bus (*GW determines what programs needed to be*

started on the target machine to create the desired workload, col. 8 lines 45-50, fig. 6a).

In regard to claim 12, Singh et al. disclosed the device of claim 11 wherein preventing the sequencer from entering a reselection phase comprises preventing the sequencer from entering a reselection phase to establish a connection to transfer data (*GW determines what programs needed to be started on the target machine to create the desired workload, col. 8 lines 45-50, fig. 6a).*

In regard to claim 13, Singh et al. disclosed the device of claim 11 wherein preventing the sequencer from entering a reselection phase comprises preventing the sequencer from entering a reselection phase to establish a connection to transfer a status (*GW determines what programs needed to be started on the target machine to create the desired workload, col. 8 lines 45-50, fig. 6a).*

In regard to claim 15, Singh et al. disclosed the device of claim 14 wherein the processor-executable instructions further comprise instructions for instructing the sequencer to enter an indefinite loop after executing the command (*an injected fault may cause the workload on the target machine to hang and produce no response, col. 13 lines 35-40).*

In regard to claim 16, Singh et al. disclosed the device of claim 10 wherein the processor-executable instructions further comprise instructions for replacing a command with an illegal command (*FIIntercept:inject(), fig. 2b).*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Singh et al. (US 6,484,276) in further view of Eckenrode et al. (US 5,363,379).

In regard to claim 9, Singh et al. does not teach the method of claim 8 wherein executing a set of instructions further comprises modifying at least some of the data in the transfer buffer so that the data contains at least one error.

Eckenrode et al. teach the FDDI network test adapter error injection circuit wherein the data error injection frame is sent out to the media (*col. 3 lines 16-33).*

It would have been obvious to modify the method of Singh et al. by adding Eckenrode et al. FDDI network test adapter error injection circuit. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would aid in detecting errors of incoming frames so that higher layers of software can tell if any errors occurred during frame transmission and reception *(col. 1 lines 65-67 and col. 2 lines 1-2).*

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 19 is rejected under 35 U.S.C. 102(b) as being anticipated by Eckenrode et al. (US 5,363,379).

In regard to claim 19, Eckenrode et al. disclosed a method comprising:

receiving a command to generate a false data miscompare error (*error injection scheme, fig. 1)*;

reading data from a storage medium into a memory (*Ram buffer access by RBC/DPC, fig. 1, 22)*;

changing at least some of the data in the memory to form corrupted data (*switching transfer data from Shadow Ram with data in Error injection Ram, col. 3 lines 16-33)*; and

passing the corrupted data as the data read from the storage medium (*Error injection data is sent out to the media, col. 3 lines 16-33).*

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 20-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Dennis et al. (US 5,471,564).

In regard to claim 20, Dennis et al. disclosed a method comprising:

receiving an indication that a false timeout error should be generated during execution of a command (*host computer system indicate a timeout period as an error condition, col. 24, lines 35-58)*;

receiving the command (*printer and other peripheral process data, col. 24 lines 35-40)*;

processing a portion of the command (*printer is out of communication with the host computer for more than the predetermine amount of time, col. 24 lines 35-58)*; and

stopping the processing of the command before completing the command without indicating that processing of the command has stopped (*generates an error message any time the arbitrary timeout period is exceeded, col. 24 lines 35-58).*

In regard to claim 21, Dennis et al. disclosed the method of claim 20 wherein receiving a command comprises receiving a read command and wherein processing a portion of the command comprises transferring data (*processing data, col. 24 lines 35-58).*

In regard to claim 22, Dennis et al. disclosed a method comprising:

receiving a command at a storage device to generate a false error, the command comprising at least one sense parameter (*host computer system indicate a timeout period as an error condition, col. 24, lines 35-58)*;

generating a false error message from the storage device that indicates that an error has occurred when it has not occurred (*in the case of the timeout period expire, the host computer will generate a false error message, col. 24 lines 35-58)*, the false error message describing the error in part by including the at least one sense parameter (*timeout, col. 24 lines 35-58).*

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Loan Truong whose telephone number is (571) 272-2572. The examiner can normally be reached on M-F from 8am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SCOTT BADERMAN
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